REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated July 31, 2002. Appreciation is expressed to the Examiner for the indication of allowable subject matter in claim 7.

By the present amendment, the title has been amended to be more descriptive of the claimed invention, as required in paragraph 2 of the Office Action. Also, claim 7 has been rewritten into independent form to place it in condition for allowance in light of the indication of allowable subject matter set forth in paragraph 25 of the Office Action. In addition, claim 14 has also been rewritten into independent form, with the subject matter of its parent claim 8 being amended to provide clear antecedent basis to overcome the 35 U.S.C. 112, second paragraph, rejection set forth in paragraphs 4-6 of the Office Action. Appreciation is expressed to the Examiner for the comments set forth in paragraph 6 regarding the necessary correction to the language of claim 8 in order to overcome this 35 U.S.C. 112, second paragraph, rejection. All other claims have been cancelled without prejudice to the applicants' right to file either a continuation or a divisional application directed to the subject matter of these cancelled claims.

With regard to claim 14, it is noted that the sole basis for rejection of the claim in the Office Action is the 35 U.S.C. 112, second paragraph, rejection set forth in paragraphs 4 – 6 of the Office Action. In other words, no prior art rejection has been made with regard to the subject matter of claim 14. It is also noted that the subject matter of claim 14 is similar to that of claim 7, indicated as containing allowable subject matter. Accordingly, in light of the amending of claim 14 into independent

form with the appropriate corrections being made to the subject matter of the language incorporated from claim 8, and in light of the fact that no prior art rejection has been made against claim 14, allowance of claim 14 is also respectfully requested. Incidentally, with regard to both claims 7 and 14, it is noted that all limitations from their various parent claims have been incorporated thereinto.

Attached hereto is a marked-up version of the changes made to the title, claims and abstract by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.39879X00).

Respectfully submitted,

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By _____
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703/312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

The title has been amended as follows:

-- NONVOLATILE SEMICONDUCTOR MEMORY DEVICE [AND PROCESS FOR PRODUCING THE SAME] WITH IMPROVED GATE OXIDE FILM ARRANGEMENTS --

In the Claims:

Claims 1-6, 8-13 and 15-42 have been cancelled without prejudice.

Claims 7 and 14 have been amended as follows:

7. (Amended) The memory device [according to claim 6] comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in a semiconductor substrate, a second diffusion layer formed in said second well and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by a shallow groove isolation method, and at least one of said

gate insulating films of said plurality of second MOS field effect transistors comprises a first insulating film deposited on the semiconductor substrate,

wherein the interpoly dielectric film comprises a second deposited insulating film which is substantially equal to said first insulating film in thickness,

wherein said first and second insulating films are a silicon oxide film,

wherein nitrogen is introduced into said silicon oxide film, and

wherein the nitrogen concentration in said second insulating film is higher than that in the first insulating film.

14. (Amended)The memory device [according to claim 13] comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said well with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first gate insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second gate insulating film which is greater than said first gate insulating film in thickness,

wherein isolation in said peripheral circuit region is effected by a shallow groove isolation method, and said second gate insulating film comprises a

first insulating film deposited on the semiconductor substrate.

wherein each of the interpoly dielectric film and the first gate insulating film comprises a second deposited insulating film,

wherein both of the first and second insulating film are a silicon oxide film,

wherein nitrogen is introduced into the silicon oxide film, and

wherein the nitrogen concentration in the films is higher in the order of interpoly dielectric film, first gate insulating film and second gate insulating film.

In the Abstract:

The abstract has been amended as follows:

ABSTRACT OF THE DISCLOSURE

[The present invention is envisioned to realize miniaturization, low voltage operation and high reliability of a nonvolatile semiconductor memory device, and simplification of its production process.] In a nonvolatile semiconductor memory device, an interpoly [Interpoly] dielectric film [109a of the nonvolatile semiconductor memory device is] composed of a nitrogen-introduced CVD SiO_2 film[, and] is used as the gate oxide [film] films of MOS transistors in [the] a low voltage region of a [the] peripheral circuit region. Gate oxide [film] films of MOS transistors in [the] a high voltage region of the peripheral circuit region [is] are composed of a laminate of [said] the SiO_2 film [109a] and a nitrogen-introduced CVD SiO_2 film. [According to the present invention,] This arrangement improves transistor characteristics and reliability of gate oxide [film] films of the peripheral circuit MOS transistors [of the nonvolatile semiconductor memory device and its transistor characteristics are improved]. It is also possible to realize miniaturization and low voltage operation [of the nonvolatile semiconductor memory device]. Further, simplification of [its] the production process is made possible.